#### card of course

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| Subject name | Foundations of digital technology |

1. The placement of the subject in the study system

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| 1.1. Field of study | Computer science |
| 1.2. Form and path of study | Full-time/Part-time |
| 1.3. Level of education | First-cycle studies |
| 1.4. Study profile | Practical |

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| 1. 5. Specialty | - |
| 1.6. Subject Coordinator | mgr Arkadiusz Gwarda |

2. General characteristics of the subject

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| 2.1. Belonging to a subject group | Directional/Practical |
| 2.2. Number of ECTS | 4 |
| 2.3. Language of lectures | Polish |
| 2.4. Semesters in which the subject is taught | I |
| 2.5.Criteria for selecting course participants | - |

1. Learning outcomes and course delivery
	1. Subject Objectives

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| No. | Subject Objectives |
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| C1 | To introduce students to the concepts of digital combinational and sequential circuits. |
| C2 | Acquiring skills in designing digital combinational circuits. |
| C3 | Acquiring skills in designing digital sequential circuits. |
| C4 | Obtaining knowledge regarding the use of digital function blocks. |

* 1. Subject-specific learning outcomes, divided into knowledge , skills and competences , with reference to the directional learning outcomes

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| No. | Description of subject learning outcomes | Reference to directional effectslearning (symbols) | Method of implementation (mark "X") |
| ST | NST |
| Classes at the University | Activities on the platform | Classes at the University | Activities on the platform |
| After passing the course, the student knows and understands **the knowledge** |
| W1 | Logic gate construction, TTL and CMOS technology | INF\_W01 INF\_W06 | X |  |  | X |
| W2 | Types and application of logic gates in digital combinational circuits | X |  |  | X |
| W3 | Types and methods of using flip-flops in digital sequential circuits | X |  |  | X |
| W4 | Types and methods of using digital function blocks, i.e.: multiplexer, demultiplexer, adder, encoder, decoder, comparator, register, counter. | X |  |  | X |
| After passing the course, the student is **able** to: |
| U1 | Perform mathematical operations using the binary number system | INF\_U05INF\_U21INF\_U22 | X |  | X |  |
| U2 | Design basic combinational circuits using digital logic gates | X |  | X |  |
| U3 | Design basic sequential circuits using flip-flops | X |  | X |  |
| U4 | Design basic digital circuits using function blocks | X |  | X |  |
| After completing the course, the student is ready to take part in **social competences.** |
| K1 | Critically evaluate the results of your work in the field of preparing digital systems and take responsibility for it | INF\_K01 | X |  | X |  |

* 1. Forms of teaching and their number of hours - Full-time studies (ST), Part-time studies (NST), Part-time PUW studies (NST PUW)

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| Path | Lecture | Exercises | Design | Workshop | Laboratory | Seminar | Lecturer | Classes conducted using distance learning methods and techniques in the form of a lecture | Other | **ECTS points** |
| **ST** | 15 |  |  |  | 30 |  |  |  |  | 4 |
| **NST** |  |  |  |  | 15 |  |  | 10 |  | 4 |

3.4. Content of education (separately for each form of classes: (W, ĆW, PROJ, WAR, LAB, LEK, OTHER). It should be marked (X) how the given content will be implemented (classes at the university or classes on the e-learning platform conducted using distance learning methods and techniques)

TYPE OF CLASS: LECTURE

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| No. | Content of the course | Reference to subject-specific learning outcomes | Method of implementation (mark "X") |
| ST | NST |
| **Classes at the University** | **Activities on the platform** | **Classes at the University** | **Activities on the platform** |
| 1. | Introduction to the subject. Basic definitions related to digital technology. Number systems. Boolean algebra. Mathematical operations in the binary system. Transistor structure of a logical gate. Types of logical gates. Ways of representing a Boolean function. | W1 | X |  |  | X |
| 2. | Combinational circuits. Design methods for simple combinational circuits. Minimization of combinational circuits. Gate circuit notation. Hazard phenomenon in digital circuits. | W2 | X |  |  | X |
| 3. | Functional blocks: multiplexers, demultiplexers, adders, subtractors, encoders, decoders, transcoders, comparators. | W4 | X |  |  | X |
| 4. | Sequential circuits. Basic definitions. Asynchronous and synchronous circuits. Types of flip-flops. Design methods for simple sequential circuits. | W3 | X |  |  | X |
| 5. | Function blocks: registers and counters.  | W4 | X |  |  | X |
| 6. | Summary of classes and discussion of grades. |  | X |  |  | X |

TYPE OF CLASS: LABORATORY

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| No. | Content of the course | **Reference to subject-specific learning outcomes** | Method of implementation (mark "X") |
| ST | NST |
| **Classes at the University** | **Activities on the platform** | **Classes at the University** | **Activities on the platform** |
| 1. | Mathematical operations in the binary number system. Representing a boolean function on logical gates. Minimizing a function using the Karnaugh table method.  | U1 | X |  | X |  |
| 2. | Combinational Design and Simulation: Adders and Encoders. | U2, U4 | X |  | X |  |
| 3. | Design and simulation of combinational circuits: . Comparators and multipliers. | U2, U4 | X |  | X |  |
| 4. | Design and simulation of sequential circuit. Flip-flops: RS, D, T, JK, JK-MS. | U3, U4 | X |  | X |  |
| 5. | Design and simulation of sequential circuit. Counters and registers. | U3, U4 | X |  | X |  |
| 6. | Summary of classes and discussion of grades. |  | X |  | X |  |

3.5. Methods of verifying learning outcomes (indicating and describing methods of conducting classes and verifying the achievement of learning outcomes, e.g. debate, case study, preparation and defense of a project, complex multimedia presentation, solving problem-solving tasks, situation simulations, study visit, simulation games + description of a given method):

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| Subject Effects | Teaching methods | Methods of verifying learning outcomes | Documentation methods |
| KNOWLEDGE |
| W1-W4 | Lecture with the use of a multimedia presentation. | Lecture credit: Written exam | Graded exam |
| SKILLS |
| U1-U4 | Solving short design tasks | Colloquium consisting of tasks resulting from the laboratory content: binary calculations, Boolean functions, logical gates, combinational and sequential circuits. | PUW Platform |
| SOCIAL COMPETENCES |
| K1 | Solving short design tasks | Colloquium consisting of tasks resulting from the laboratory content: binary calculations, Boolean functions, logical gates, combinational and sequential circuits. | PUW Platform |

3.6. Assessment criteria for the achieved learning outcomes

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| Learning effect | For a grade of 3 or "pass."the student knows and understands/is able to/is ready to | For a grade of 3.5, the student knows and understands/is able to/is ready to | For a grade of 4, the student knows and understands/is able to/is ready to | For a grade of 4.5, the student knows and understands/is able to/is ready to | For a grade of 5, the student knows and understands/is able to/is ready to |
| W | 51-60% of knowledge indicated in learning outcomes | 61-70% of knowledge indicated in learning outcomes | 71-80% of knowledge indicated in learning outcomes | 81-90% of knowledge indicated in learning outcomes | 91-100% of knowledge indicated in learning outcomes |
| U | 51-60% of skills indicated in learning outcomes | 61-70% of skills indicated in learning outcomes | 71-80% of skills indicated in learning outcomes | 81-90% of skills indicated in learning outcomes | 91-100% of skills indicated in learning outcomes |
| K | 51-60% of skills indicated in learning outcomes | 61-70% of skills indicated in learning outcomes | 71-80% of skills indicated in learning outcomes | 81-90% of skills indicated in learning outcomes | 91-100% of skills indicated in learning outcomes |

3.7. Literature

**Basic**

1. A. Skorupski – Podstawy techniki cyfrowej, WKŁ 2004
2. T. Łuba – Synteza układów logicznych, WPW 2005
3. C. Zieliński – Podstawy projektowania układów cyfrowych, PWN 2003

**Supplementary**

1. Technika cyfrowa : zbiór zadań z rozwiązaniami, Jerzy Tyszer, Grzegorz Mrugalski, Artur Pogiel, Dariusz Czysz, - Wyd. 2. zm. Legionowo : Wydawnictwo BTC, 2016

4. Student workload - ECTS points balance

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| **Types of student activity** | **Student Load** |
| **ST** | **NST** |
| **Classes requiring direct contact between the student and the academic teacher at the university premises** | **45** | **25** |
| Classes included in the study plan | 45 | 25 |
| **Student's own work** | **55** | **75** |
| Ongoing preparation for classes, preparation of project work/presentations/etc. | 30 | 35 |
| Preparation for passing classes | 25 | 40 |
| **TOTAL STUDENT HOURLY LOAD** | **100** | **100** |
| **Number of ECTS points** | **4** | **4** |

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| Last change date | 30/09/2024 |
| The changes were introduced | INF Education Quality Team |
| The changes were approved | Arkadiusz Gwarda, M.A. |